

INSTANTANEOUS
OUTPUT POWER
(dBm)

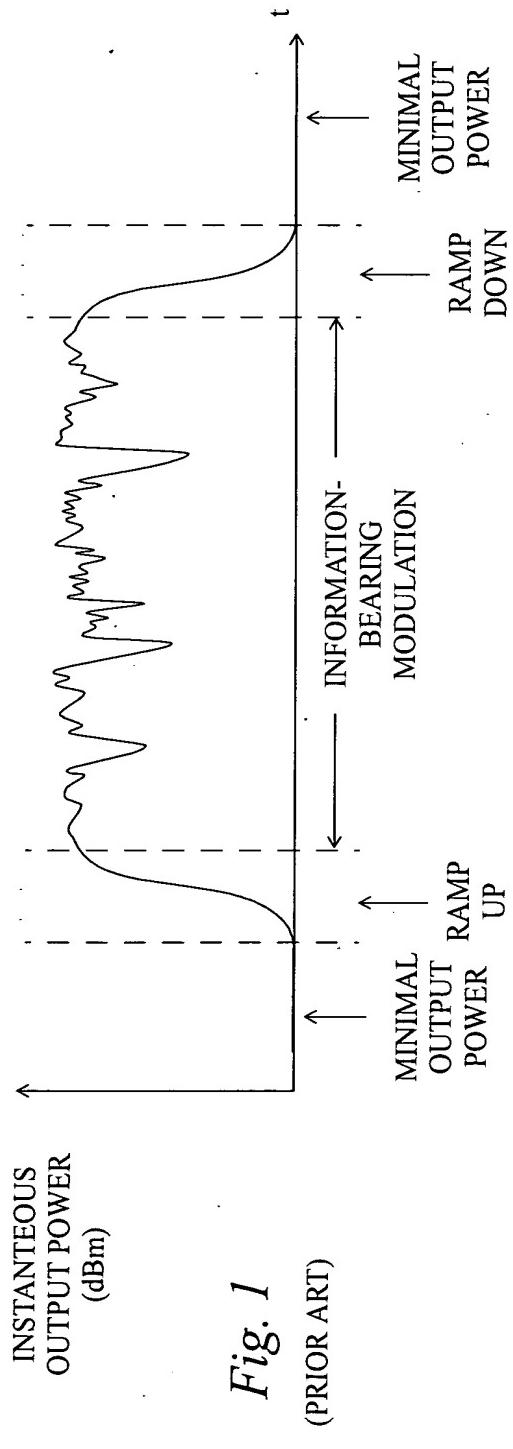


Fig. 13
(PRIOR ART)

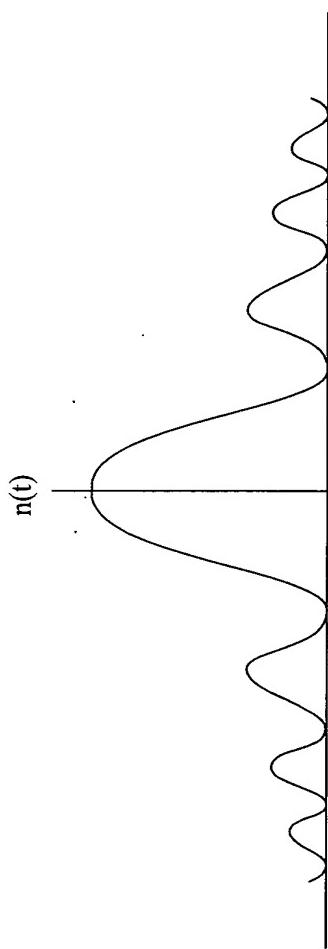


Fig. 2
(PRIOR ART)

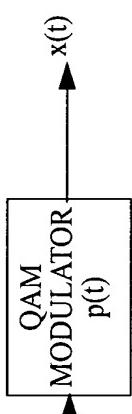


Fig. 3
(PRIOR ART)

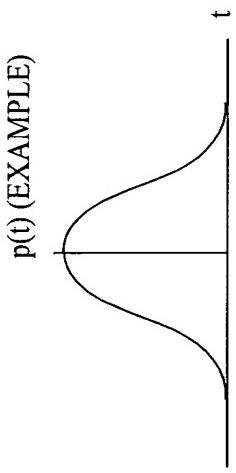


Fig. 4

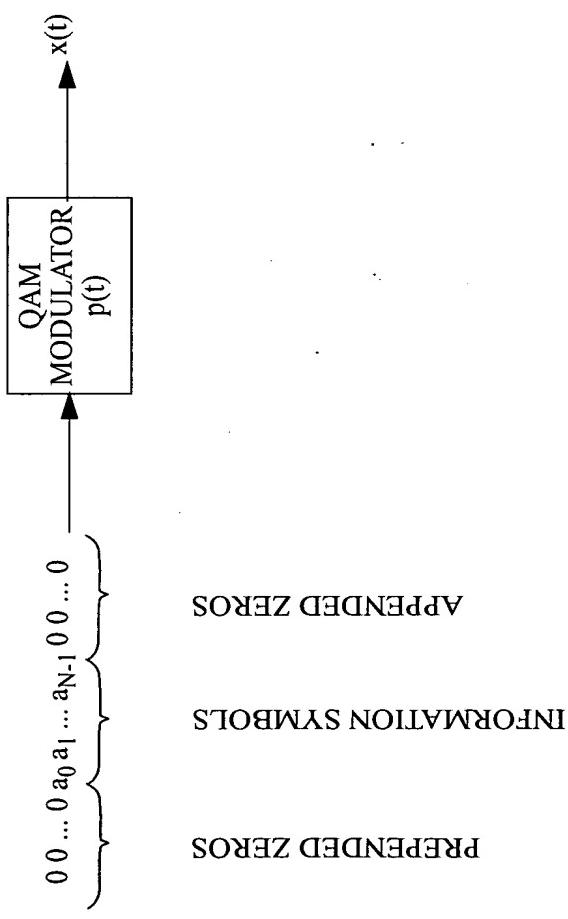


Fig. 5

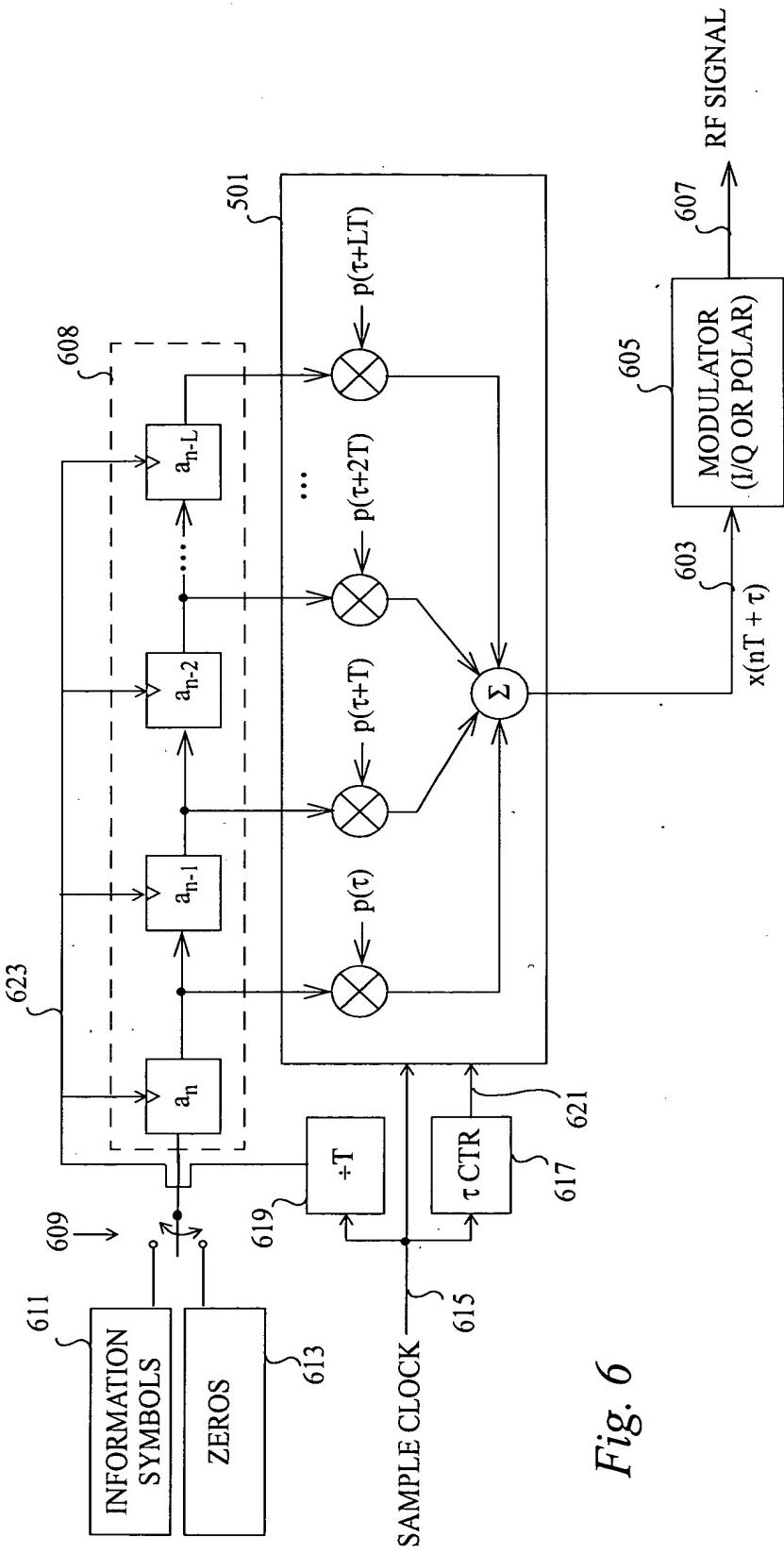
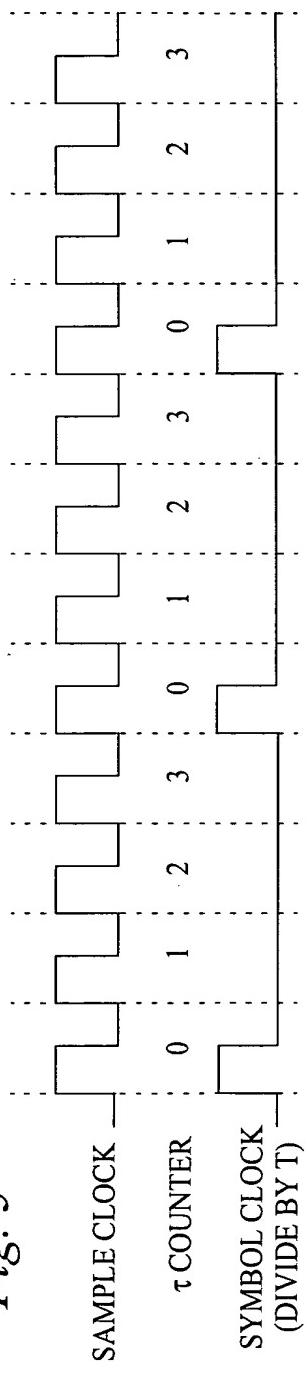


Fig. 6

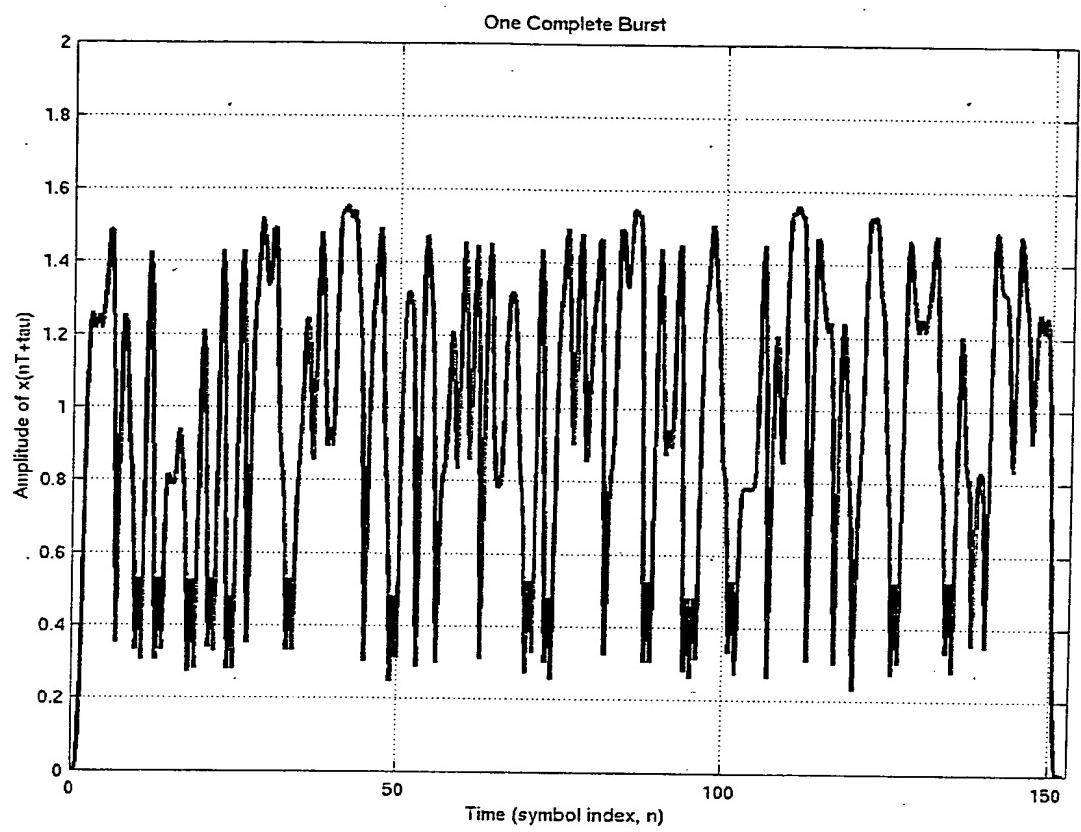


Fig. 7

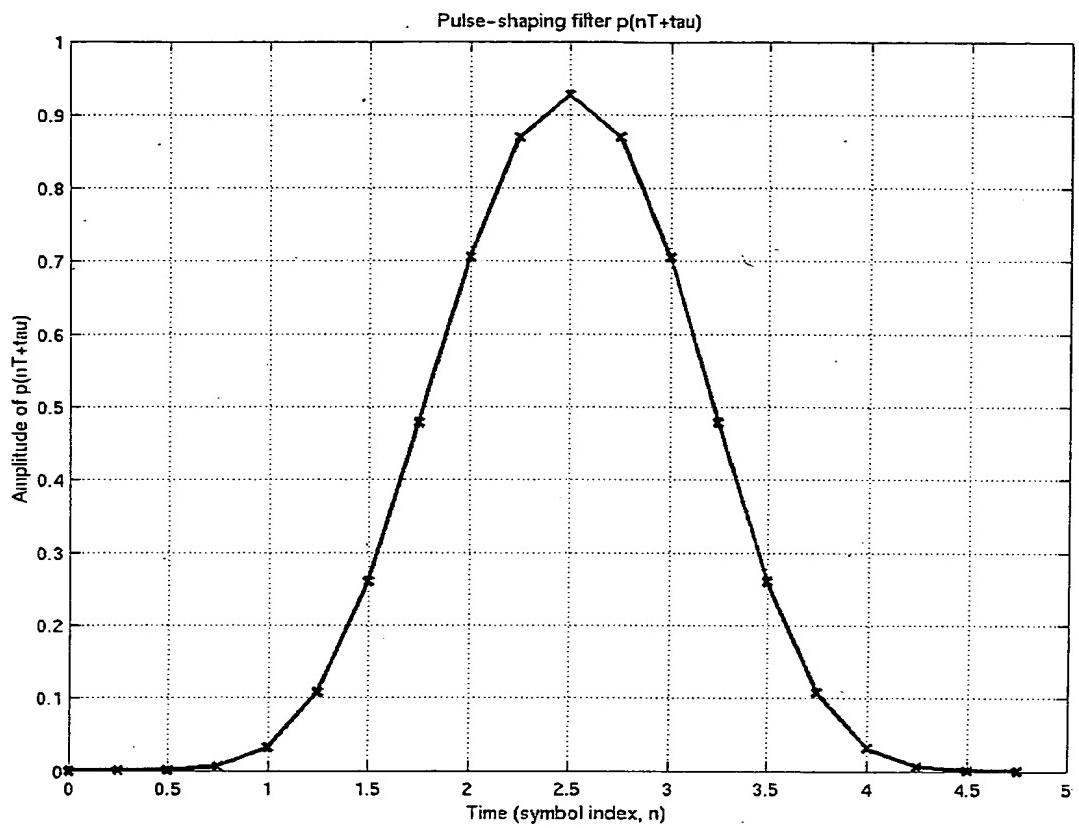
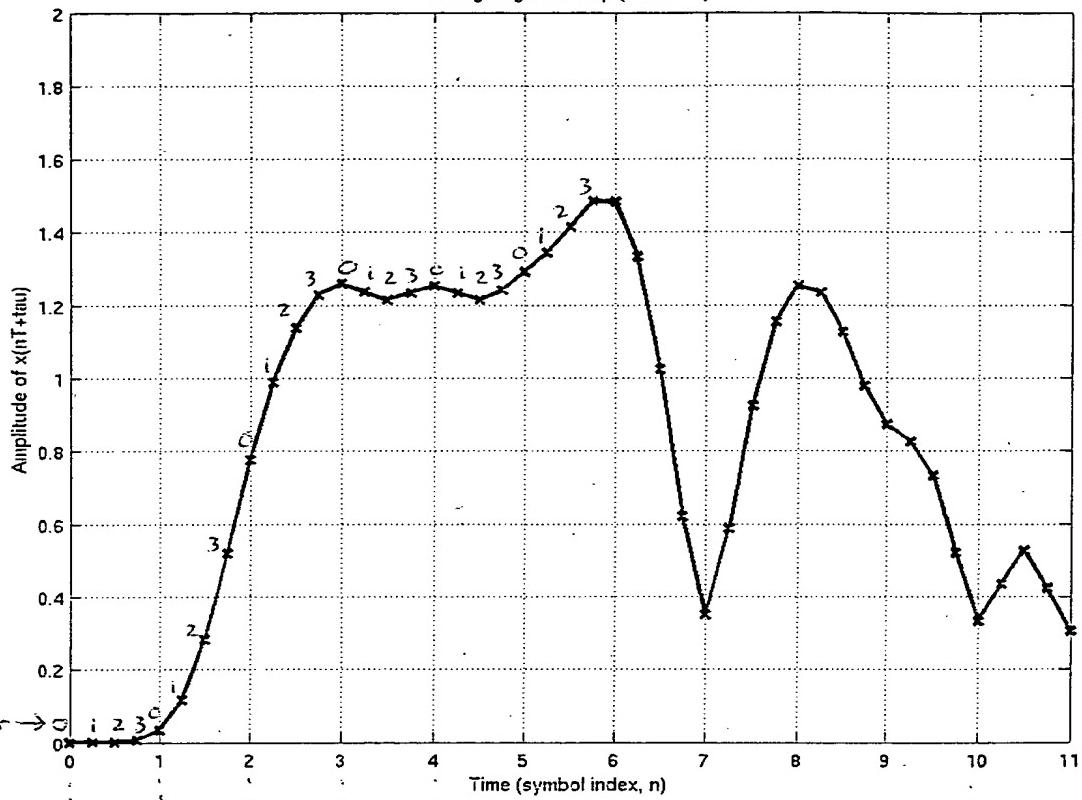


Fig. 8

Rising Edge of Ramp (with T=4)



Shift register contents

a_n	a_0	a_1	a_2	a_3	a_4	a_5	\dots	a_{10}
a_{n-1}	0	a_0	a_1	a_2	a_3	a_4	\dots	a_9
a_{n-2}	0	0	a_0	a_1	a_2	a_3	\dots	a_8
a_{n-3}	0	0	0	a_0	a_1	a_2	\dots	a_7
a_{n-4}	0	0	0	0	a_0	a_1	\dots	a_6

Fig. 9

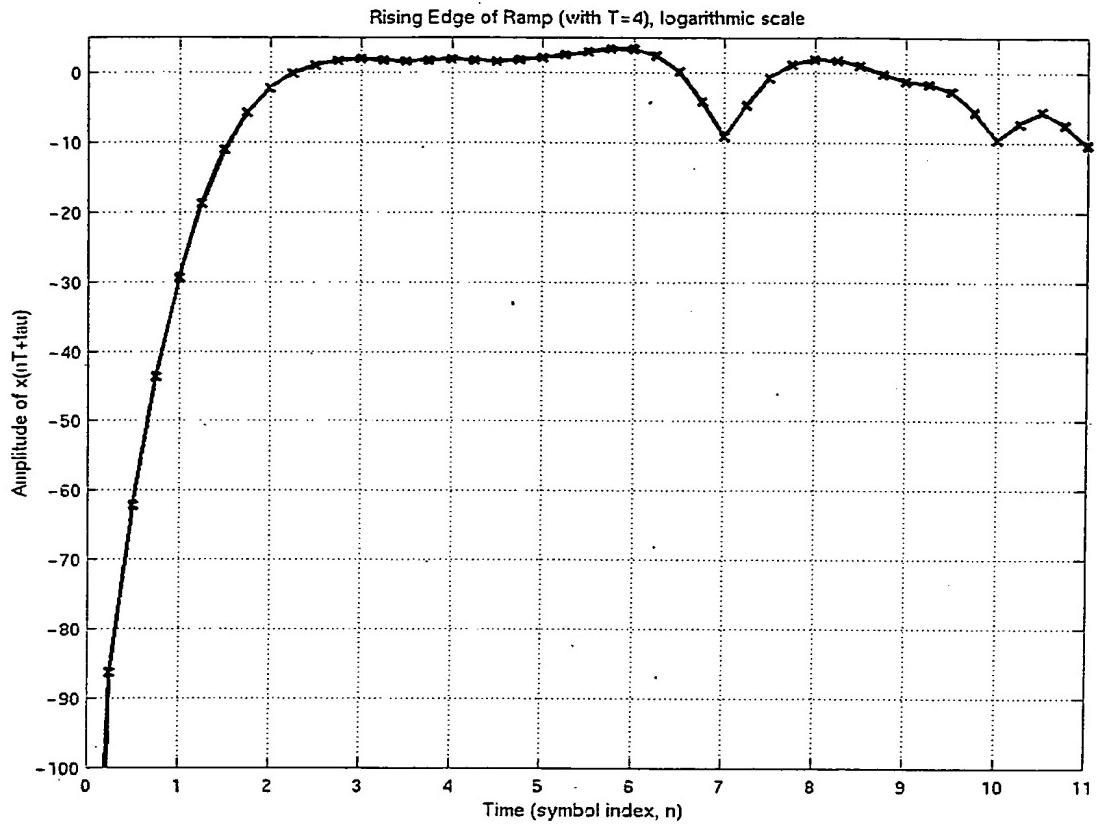
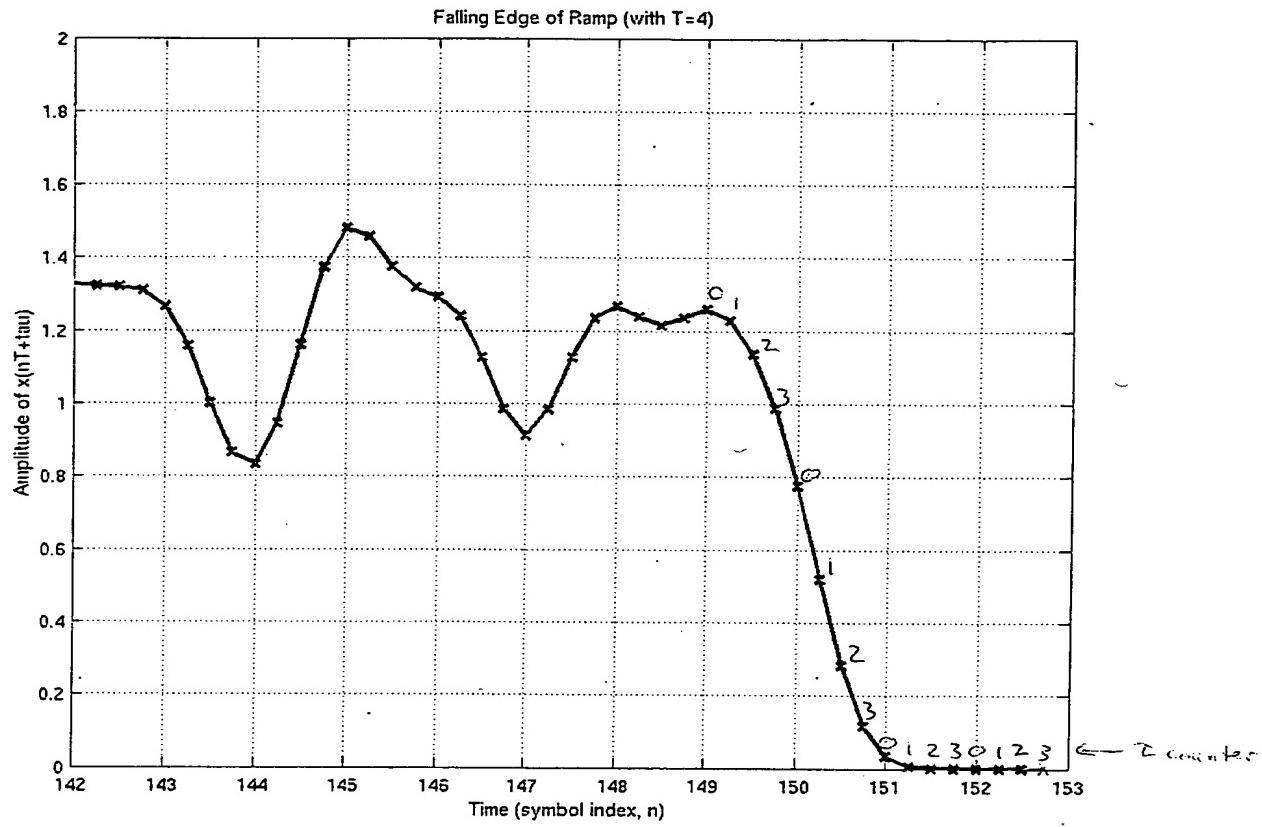


Fig. 10



Shift

register
contents

a_n	a_{142}	a_{141}	a_{140}	a_{139}	a_{138}	a_{146}	a_{147}	0	0	0	0	0
a_{n-1}	a_{141}	\sim	\sim	\sim	\sim	a_{145}	a_{146}	a_{147}	0	0	0	0
a_{n-2}	a_{140}					a_{144}	a_{145}	a_{146}	a_{147}	0	0	0
a_{n-3}	a_{139}					a_{143}	a_{144}	a_{145}	a_{146}	a_{147}	0	0
a_{n-4}	a_{138}	\sim	\sim	\sim	\sim	a_{142}	a_{143}	a_{144}	a_{145}	a_{146}	a_{147}	0

Fig. 11

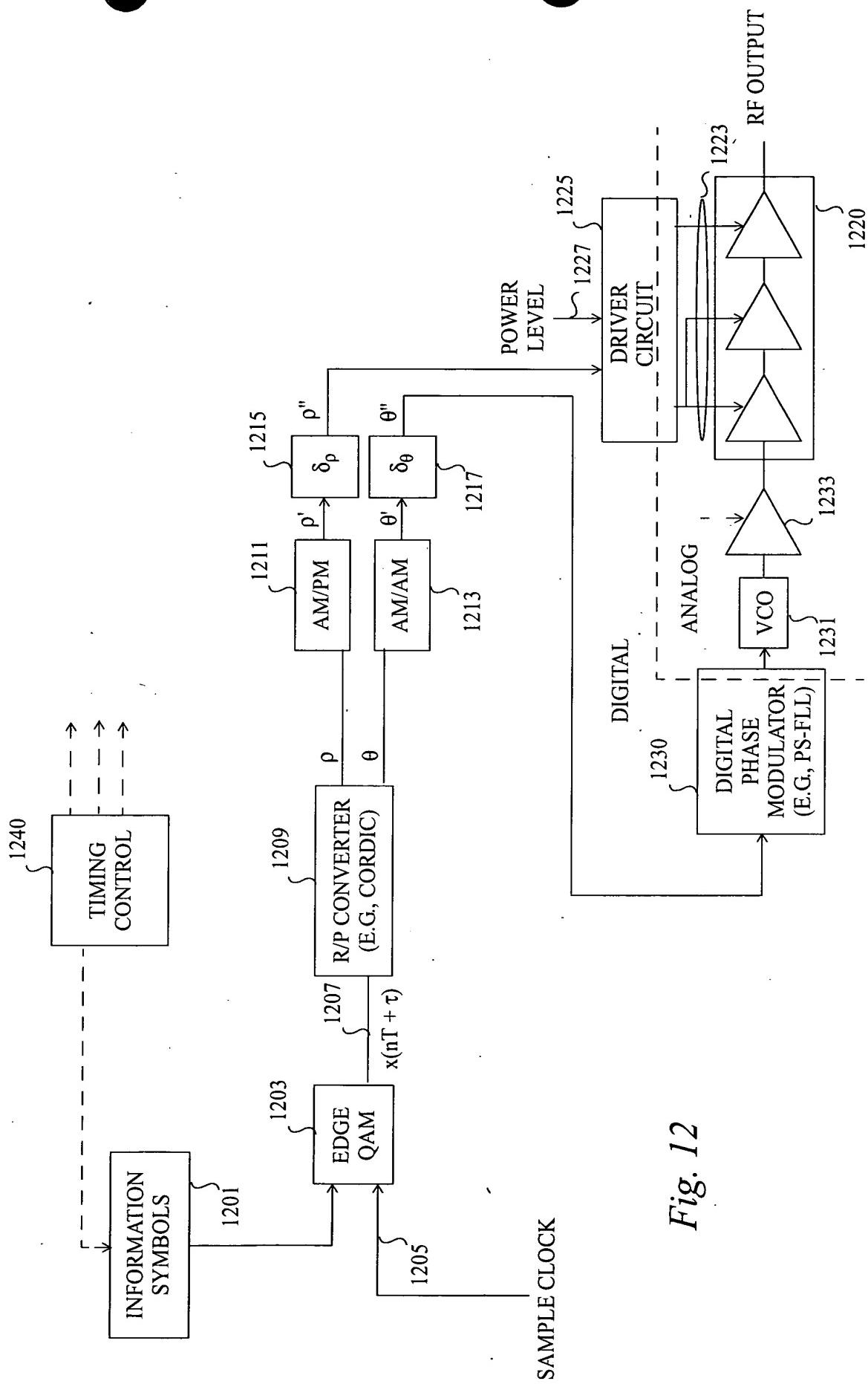


Fig. 12

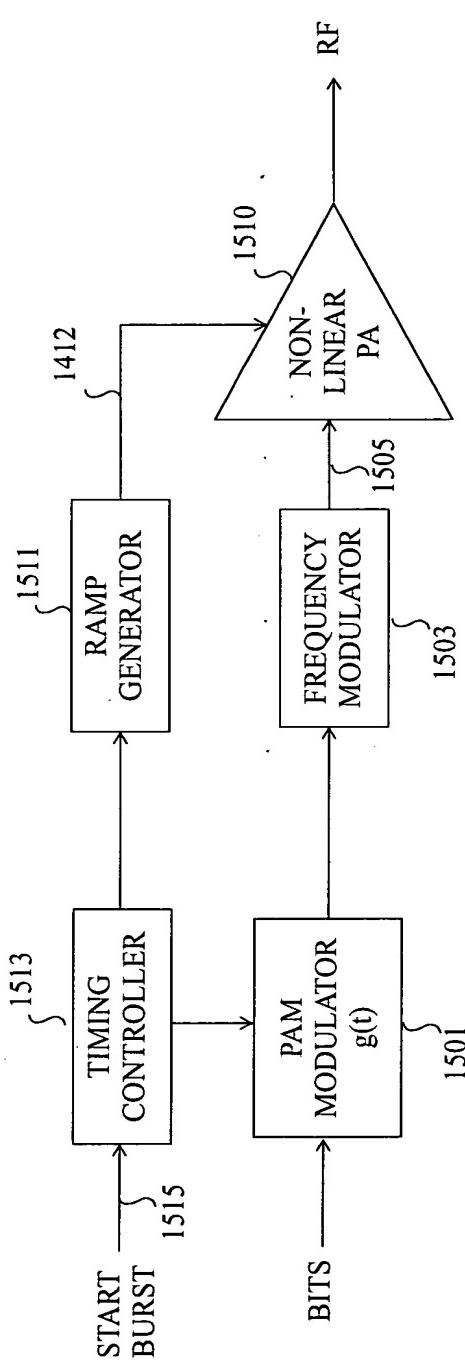


Fig. 15

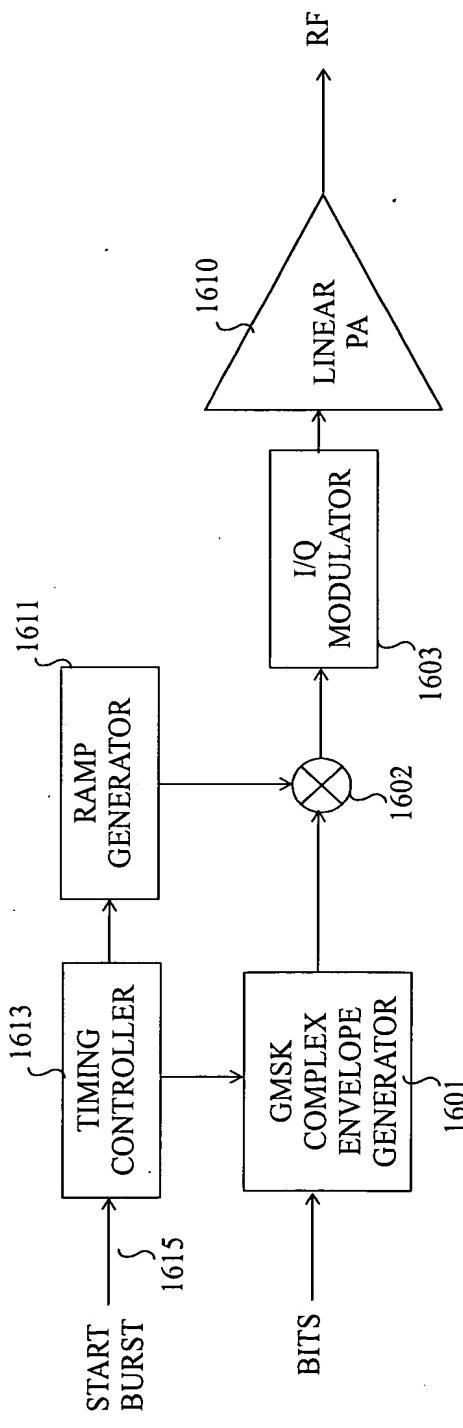


Fig. 16

Fig. 14

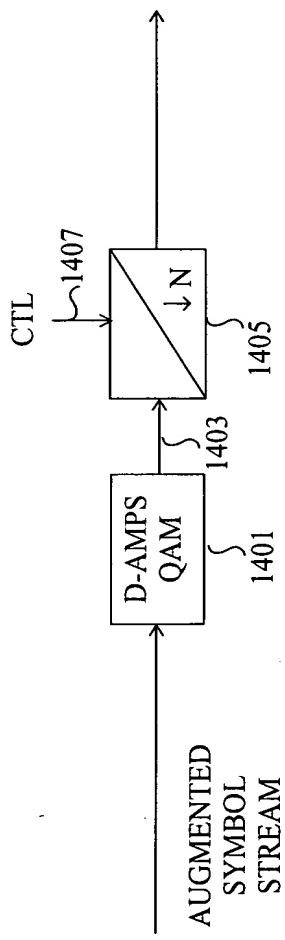


Fig. 14

“RAMPED-UP STATE”
(INFORMATION BITS
TRANSMITTED)

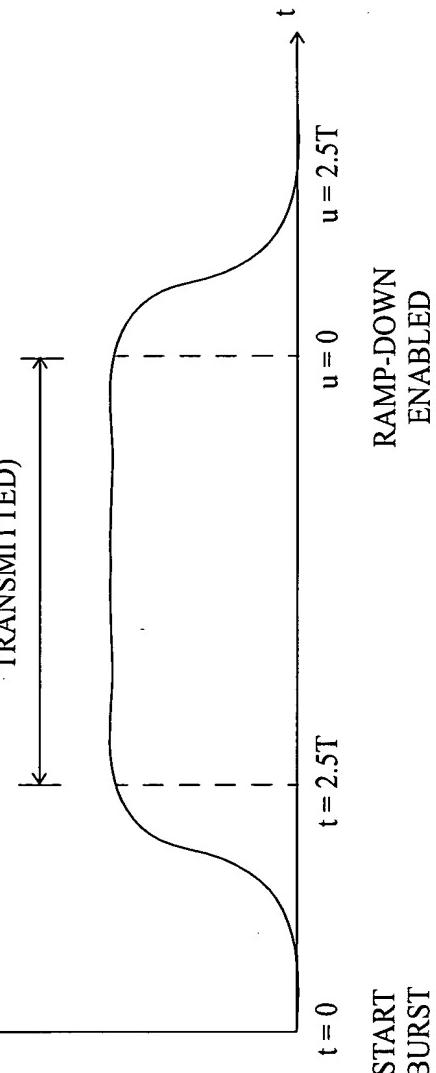


Fig. 17

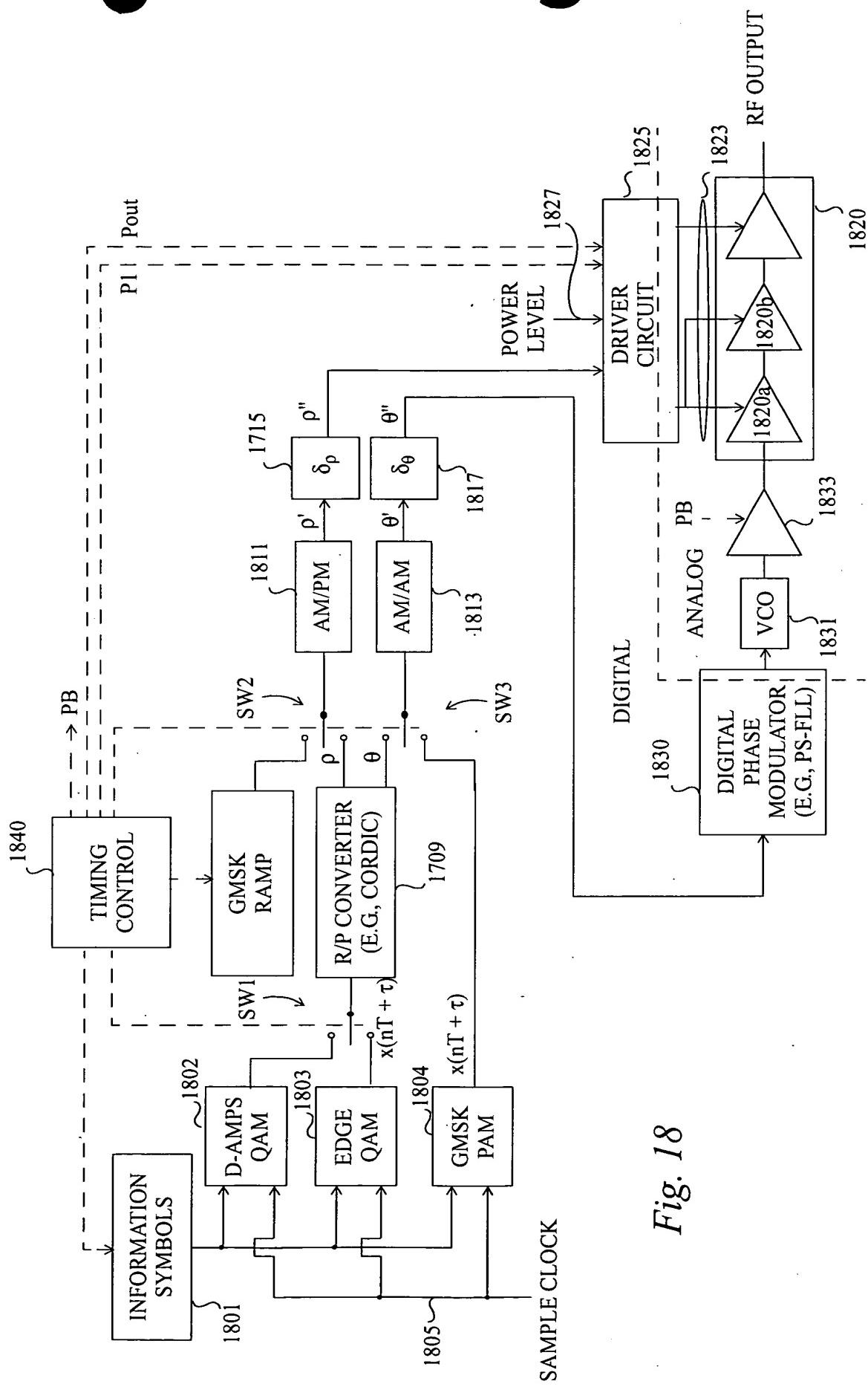


Fig. 18

“RAMPED-UP STATE”
(INFORMATION BITS
TRANSMITTED)

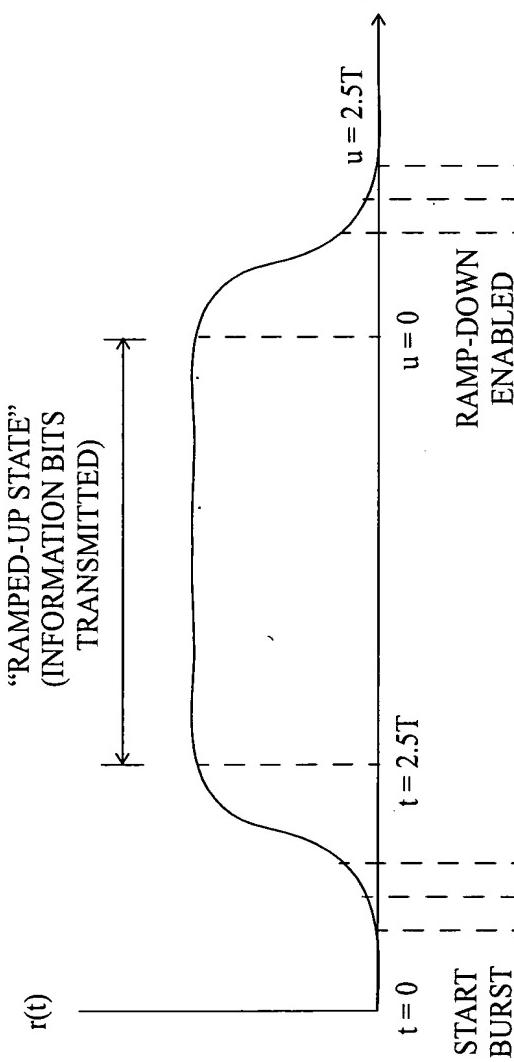


Fig. 19

